

What is claimed is:

1 1. An interconnect structure, comprising:
2 a lower level wire having a side and a bottom, said
3 lower level wire comprising a lower core conductor and a
4 lower conductive liner, said lower conductive liner on the
5 side and the bottom of said lower level wire;
6 an upper level wire having a side and a bottom, said
7 upper level wire comprising an upper core conductor and an
8 upper conductive liner, said upper conductive liner on the
9 side and the bottom of said upper level wire; and
10 said upper conductive liner in contact with said lower
11 core conductor and also in contact with said lower
12 conductive liner in a liner-to-liner contact region.

1 2. The interconnect structure of claim 1, wherein said
2 lower level wire is formed by a damascene process in a lower
3 level dielectric and said upper level wire is formed by a
4 damascene process in an upper level dielectric.

1 3. The interconnect structure of claim 1, wherein said
2 upper and lower core conductors are selected from the group

3 consisting of copper, aluminum, aluminum-copper and
4 aluminum-copper-silicon.

1 4. The interconnect structure of claim 1, wherein said
2 upper and lower conductive liners are selected from the
3 group consisting of tantalum, tantalum nitride, titanium,
4 titanium nitride, tungsten and combinations thereof.

1 5. The interconnect structure of claim 1, wherein said
2 lower conductive liner includes an upper edge having an
3 inner surface, an outer surface, and a top surface and said
4 upper conductive liner contacts one or more of said inner,
5 outer and top surfaces to form said liner-to-liner contact
6 region.

1 6. The interconnect structure of claim 1, wherein said
2 liner-to liner contact region comprises a first portion co-
3 extensive with said lower conductive liner on a portion of a
4 first side of said lower level wire under said upper level
5 wire.

1 7. The interconnect structure of claim 6, wherein said
2 liner-to liner contact region further comprises a second
3 portion co-extensive with said lower conductive liner on a
4 portion of a second side of said lower level wire under said
5 upper level wire.

1 8. The interconnect structure of claim 7, wherein said
2 liner-to-liner contact region further comprises a third
3 portion co-extensive with said lower conductive liner on an
4 end of said lower level wire under said upper level wire.

1 9. The interconnect structure of claim 2, wherein said
2 first and second dielectrics are selected from the group
3 consisting of silicon oxide, silicon nitride, diamond,
4 fluorine doped silicon oxide, spin on glass, porous silicon
5 oxide, polyimide, polyimide siloxane, polysilsequioxane
6 polymer, benzocyclobutene, paralyene N, paralyene F,
7 polyolefin, poly-naphthalene, amorphous Teflon, SILK™,
8 black diamond, polymer foam, aerogel, air, dielectric gases,
9 a partial vacuum and combinations thereof.

1 10. An interconnect structure, comprising:
2 a lower level wire having a side and a bottom, said
3 lower level wire comprising a lower core conductor and an
4 lower conductive liner, said lower conductive liner on the
5 side and the bottom of said lower level wire;
6 an upper level wire having a side and a bottom and a
7 via integrally formed in the bottom of said upper level
8 wire, said via have a side and a bottom, said upper level
9 wire and said via each comprising an upper core conductor
10 and an upper conductive liner, said upper conductive liner
11 on the side and the bottom of said upper level wire and on
12 the side and bottom of said via; and
13 said upper conductive liner on the bottom of said via
14 in contact with said lower core conductor and also in
15 contact with said lower conductive liner in a liner-to-liner
16 contact region.

1 11. The interconnect structure of claim 10, wherein
2 said lower level wire is formed by a damascene or dual
3 damascene process in a lower level dielectric and said upper
4 level wire is formed by a dual-damascene process in an upper
5 level dielectric.

1 12. The interconnect structure of claim 10, wherein
2 said upper and lower core conductors are selected from the
3 group consisting of copper, aluminum, aluminum-copper and
4 aluminum-copper-silicon.

1 13. The interconnect structure of claim 10, wherein
2 said upper and lower conductive liners are selected from the
3 group consisting of tantalum, tantalum nitride, titanium,
4 titanium nitride, tungsten and combinations thereof.

1 14. The interconnect structure of claim 10, wherein
2 said lower conductive liner includes an upper edge having an
3 inner surface, an outer surface, and a top surface and said
4 upper conductive liner on the bottom of said via contacts
5 one or more of said inner, outer and top surfaces to form
6 said liner-to-liner contact region.

1 15. The interconnect structure of claim 10, wherein
2 said liner-to liner contact region comprises a first portion
3 co-extensive with said lower conductive liner on a portion
4 of a first side of said lower level wire under said via.

1 16. The interconnect structure of claim 15, wherein
2 said liner-to liner contact region further comprises a
3 second portion co-extensive with said lower conductive liner
4 on a portion of a second side of said lower level wire under
5 said via.

1 17. The interconnect structure of claim 16, wherein
2 said liner-to-liner contact region further comprises a third
3 portion co-extensive with said lower conductive liner on an
4 end of said lower level wire under said via.

1 18. The interconnect structure of claim 10, wherein
2 said liner-to liner contact region comprises a first portion
3 co-extensive with said lower conductive liner on a portion
4 of a first side of said lower level wire under said via and
5 a second portion co-extensive with said lower conductive
6 liner on a portion of an end of said lower level wire under
7 said via.

1 19. The interconnect structure of claim 11, wherein
2 said first and second dielectrics are selected from the
3 group consisting of silicon oxide, silicon nitride, diamond,

1 20. An interconnect structure, comprising:
2 a lower level wire having a side and a bottom, said
3 lower level wire comprising a lower core conductor and an
4 lower conductive liner, said lower conductive liner on the
5 side and the bottom of said lower level wire;
6 an upper level wire having a side and a bottom and an
7 array of vias integrally formed in the bottom of said upper
8 level wire, each via of said array of vias having a side and
9 a bottom, said upper level wire and each via comprising an
10 upper core conductor and an upper conductive liner, said
11 upper conductive liner on the side and the bottom of said
12 upper level wire and on the side and bottom of each via; and
13 said upper conductive liner on the bottom of each via
14 of a first portion of said array of vias in contact with
15 said lower core conductor and each via of a second portion
16 of said array of vias in contact with said lower core
17 conductor and also in contact with said lower conductive
18 liner in liner-to-liner contact regions.

1 21. The interconnect structure of claim 20, wherein
2 said lower conductive liner includes an upper edge having an
3 inner surface, an outer surface, and a top surface and said

4 upper conductive liner on the bottom of vias of said second
5 portion of said array of vias contact one or more of said
6 inner, outer and top surfaces to form said liner-to-liner
7 contact region.

1 22. The interconnect structure of claim 20, wherein
2 said liner-to liner contact region comprises first portions
3 co-extensive with said lower conductive liner on portions of
4 first sides of said lower level wire under vias of said
5 second portion of said array of vias.

1 23. The interconnect structure of claim 22, wherein
2 said liner-to liner contact region further comprises second
3 portions co-extensive with said lower conductive liner on
4 portions of second sides of said lower level wire under vias
5 of said second portion of said array of vias.

1 24. The interconnect structure of claim 23, wherein
2 said liner-to-liner contact region further comprises a third
3 portion co-extensive with said lower conductive liner on an
4 end of said lower level wire under vias of said second
5 portion of said array of vias.

1 25. An interconnect structure, comprising:
2 a lower level wire having a side and a bottom and one
3 or more integral extensions each extension having a side and
4 a bottom , said lower level wire and extensions comprising a
5 lower core conductor and an lower conductive liner, said
6 lower conductive liner on the side and the bottom of said
7 lower level wire and said extensions;
8 an upper level wire having a side and a bottom and an
9 array of vias integrally formed in the bottom of said upper
10 level wire, each via of said array of vias having a side and
11 a bottom, said upper level wire and each via comprising an
12 upper core conductor and an upper conductive liner, said
13 upper conductive liner on the side and the bottom of said
14 upper level wire and on the side and bottom of each via; and
15 said upper conductive liner on the bottom of each said
16 via of a first portion of said array of vias in contact with
17 said lower core conductor of said lower level wire and a
18 second portion of said array of vias in contact with said
19 lower core conductor of said extensions and also in contact
20 with said lower conductive liner of said extensions in
21 liner-to-liner contact regions.

1 26. The interconnect structure of claim 25, wherein
2 said lower conductive liner on said extension includes an
3 upper edge having an inner surface, an outer surface, and a
4 top surface and said upper conductive liner on the bottom of
5 vias of said second portion of said array of vias contact
6 one or more of said inner, outer and top surfaces to form
7 said liner-to-liner contact region.

1 27. The interconnect structure of claim 25, wherein
2 said liner-to liner contact region comprises first portions
3 co-extensive with said lower conductive liner on portions of
4 first sides of said extensions of said lower level wire
5 under vias of said second portion of said array of vias.

1 28. The interconnect structure of claim 27, wherein
2 said liner-to liner contact region further comprises second
3 portions co-extensive with said lower conductive liner on
4 portions of second sides of said extensions of said lower
5 level wire under vias of said second portion of said array
6 of vias.

1 29. The interconnect structure of claim 28, wherein
2 said liner-to-liner contact region further comprises a third
3 portion co-extensive with said lower conductive liner on an
4 end of said lower level wire under vias of said second
5 portion of said array of vias.

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1 30. An interconnect structure, comprising:
2 a lower level wire having a side and a bottom, said
3 lower level wire comprising a lower core conductor and a
4 lower conductive liner, said lower conductive liner on the
5 side and the bottom of said lower level wire;
6 one or more dielectric pillars formed in said lower
7 level wire, said lower conductive liner on sides of said
8 dielectric pillars;
9 an upper level wire having a side and a bottom, said
10 upper level wire comprising an upper core conductor and an
11 upper conductive liner, said upper conductive liner on the
12 side and the bottom of said upper level wire; and
13 said upper conductive liner in contact with said lower
14 core conductor and also in contact with said lower
15 conductive liner on the sides of said dielectric pillars in
16 liner-to-liner contact regions.

1 31. An interconnect structure, comprising:
2 a lower level wire having a side and a bottom, said
3 lower level wire comprising a lower core conductor and an
4 lower conductive liner, said lower conductive liner on the
5 side and the bottom of said lower level wire;
6 one or more dielectric pillars formed in said lower
7 level wire, said lower conductive liner on sides of said
8 dielectric pillars;
9 an upper level wire having a side and a bottom and one
10 or more vias integrally formed in the bottom of said upper
11 level wire, each via having a side and a bottom, said upper
12 level wire and each via comprising an upper core conductor
13 and an upper conductive liner, said upper conductive liner
14 on the side and the bottom of said upper level wire and on
15 the side and bottom of each via; and
16 said upper conductive liner on the bottom of at least a
17 portion of said one or more vias in contact with said lower
18 core conductor and at least a portion of said one or more
19 vias in contact with said lower conductive liner on said
20 side of at least a portion of said one or more dielectric
21 pillars in liner-to-liner contact regions.

1 32. The interconnect structure of claim 31, wherein
2 said lower conductive liner on the side of said one or more
3 dielectric pillars includes an upper edge having an inner
4 surface, an outer surface, and a top surface and said upper
5 conductive liner on the bottom of vias of said second
6 portion of said array of vias contact one or more of said
7 inner, outer and top surfaces to form said liner-to-liner
8 contact region.

1 33. The interconnect structure of claim 31, wherein
2 said liner-to liner contact region comprises first portions
3 co-extensive with said lower conductive liner on portions of
4 first sides of said dielectric pillars under said vias.

1 34. The interconnect structure of claim 33, wherein
2 said liner-to liner contact region further comprises second
3 portions co-extensive with said lower conductive liner on
4 portions of second sides of said dielectric pillars under
5 said vias.

1 35. The interconnect structure of claim 34, wherein
2 said liner-to-liner contact region further comprises a third

1 36. A method of fabricating an interconnect structure,
2 comprising:
3 providing a substrate;
4 forming, on said substrate, a lower level wire having a
5 side and a bottom, said lower level wire comprising a lower
6 core conductor and a lower conductive liner, said lower
7 conductive liner formed on the side and the bottom of said
8 lower level wire;
9 forming an upper level wire having a side and a bottom,
10 said upper level wire comprising an upper core conductor
11 and an upper conductive liner, said upper conductive liner
12 formed on the side and the bottom of said upper level wire;
13 and
14 aligning said lower level wire with said upper level
15 wire such that said upper conductive liner contacts said
16 lower core conductor and also contacts said lower conductive
17 liner to form a liner-to-liner contact region.

1 37. The method of claim 36, wherein said lower level
2 wire is formed by a damascene process in a lower level
3 dielectric layer and said upper level wire is formed by a
4 damascene process in an upper level dielectric layer.

1 38. The method of claim 36, wherein said upper and
2 lower core conductors are selected from the group consisting
3 of copper, aluminum, aluminum-copper and aluminum-copper-
4 silicon.

1 39. The method of claim 36, wherein said upper and
2 lower conductive liners are selected from the group
3 consisting of tantalum, tantalum nitride, titanium, titanium
4 nitride, tungsten and combinations thereof.

1 40. The method of claim 37, wherein said first and
2 second dielectrics are selected from the group consisting of
3 silicon oxide, silicon nitride, diamond, fluorine doped
4 silicon oxide, spin on glass, porous silicon oxide,
5 polyimide, polyimide siloxane, polysilsequioxane polymer,
6 benzocyclobutene, paralyene N, paralyene F, polyolefin,
7 poly-naphthalene, amorphous Teflon, SILK™, black diamond,
8 polymer foam, aerogel, air, dielectric gases, a partial
9 vacuum and combinations thereof.

1 41. A method of fabricating an interconnect structure,
2 comprising:
3 providing a substrate;
4 forming, on said substrate, a lower level wire having a
5 side and a bottom, said lower level wire comprising a lower
6 core conductor and an lower conductive liner, said lower
7 conductive liner formed on the side and the bottom of said
8 lower level wire in a lower dielectric layer;
9 forming an upper level wire having a side and a bottom
10 and a via integrally formed in the bottom of said upper
11 level wire, said via having a side and a bottom, said upper
12 level wire and said via each comprising an upper core
13 conductor and an upper conductive liner, said upper
14 conductive liner formed on the side and the bottom of said
15 upper level wire and on the side and bottom of said via; and
16 aligning upper level wire with said lower level wire
17 such that said upper conductive liner on the bottom of said
18 via contacts said lower core conductor and also contacts
19 said lower conductive liner to form a liner-to-liner contact
20 region.

1 42. The method of claim 41, wherein said lower level
2 wire is formed by a damascene process in a lower level
3 dielectric layer and said upper level wire is formed by a
4 damascene process in an upper level dielectric layer.

1 43. The method of claim 41, wherein said upper and
2 lower core conductors are selected from the group consisting
3 of copper, aluminum, aluminum-copper and aluminum-copper-
4 silicon.

1 44. The method of claim 41, wherein said upper and
2 lower conductive liners are selected from the group
3 consisting of tantalum, tantalum nitride, titanium, titanium
4 nitride, tungsten and combinations thereof.

1 45. The method of claim 41, wherein said first and
2 second dielectrics are selected from the group consisting of
3 silicon oxide, silicon nitride, diamond, fluorine doped
4 silicon oxide, spin on glass, porous silicon oxide,
5 polyimide, polyimide siloxane, polysilsequioxane polymer,
6 benzocyclobutene, paralyene N, paralyene F, polyolefin,
7 poly-naphthalene, amorphous Teflon, SILK™, black diamond,

- 8 polymer foam, aerogel, air, dielectric gases, a partial
- 9 vacuum and combinations thereof.

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1 46. A method of forming an interconnect structure,
2 comprising:
3 providing a substrate;
4 forming, on said substrate, a lower level wire having a
5 side and a bottom, said lower level wire comprising a lower
6 core conductor and a lower conductive liner, said lower
7 conductive liner formed on the side and the bottom of said
8 lower level wire;
9 forming one or more dielectric pillars in said lower
10 level wire, said lower conductive liner formed on sides of
11 said dielectric pillars;
12 forming an upper level wire having a side and a bottom,
13 said upper level wire comprising an upper core conductor
14 and an upper conductive liner, said upper conductive liner
15 formed on the side and the bottom of said upper level wire;
16 and
17 aligning said upper level wire with said lower level
18 wire such that said upper conductive liner contacts said
19 lower core conductor and also contacts said lower conductive
20 liner on the sides of said dielectric pillars to form liner-
21 to-liner contact regions.

1 47. A method of fabricating an interconnect structure,
2 comprising:
3 providing a substrate;
4 forming, on said substrate, a lower level wire having a
5 side and a bottom, said lower level wire comprising a lower
6 core conductor and an lower conductive liner, said lower
7 conductive liner formed on the side and the bottom of said
8 lower level wire;
9 forming one or more dielectric pillars in said lower
10 level wire, said lower conductive liner formed on sides of
11 said dielectric pillars;
12 forming an upper level wire having a side and a bottom
13 and one or more vias integrally formed in the bottom of said
14 upper level wire, each via having a side and a bottom, said
15 upper level wire and each via comprising an upper core
16 conductor and an upper conductive liner, said upper
17 conductive liner formed on the side and the bottom of said
18 upper level wire and on the side and bottom of each via; and
19 aligning said upper level wire to said lower level wire
20 such that said upper conductive liner on the bottom of at
21 least a portion of said one or more vias contacts said lower
22 core conductor and at least a portion of said one or more

23 vias contacts said lower conductive liner on said side of at
24 least a portion of said one or more dielectric pillars to
25 form liner-to-liner contact regions.

1 48. The method of claim 47, wherein said lower level
2 wire is formed by a damascene process in a lower level
3 dielectric layer and said upper level wire is formed by a
4 dual-damascene process in an upper level dielectric layer.

1 49. The method of claim 47, wherein said upper and
2 lower core conductors are selected from the group consisting
3 of copper, aluminum, aluminum-copper and aluminum-copper-
4 silicon.

1 50. The method of claim 47, wherein said upper and
2 lower conductive liners are selected from the group
3 consisting of tantalum, tantalum nitride, titanium, titanium
4 nitride, tungsten and combinations thereof.

1 51. The method of claim 47, wherein dielectric pillars
2 are formed from material selected from the group consisting
3 of silicon oxide, silicon nitride, diamond, fluorine doped

4 silicon oxide, spin on glass, porous silicon oxide,
5 polyimide, polyimide siloxane, polysilsequioxane polymer,
6 benzocyclobutene, paralyene N, paralyene F, polyolefin,
7 poly-naphthalene, amorphous Teflon, SILK™, black diamond,
8 polymer foam, aerogel, air, dielectric gases, a partial
9 vacuum and combinations thereof.

1 52. The method of claim 48, wherein said first and
2 second dielectrics are selected from the group consisting of
3 silicon oxide, silicon nitride, diamond, fluorine doped
4 silicon oxide, spin on glass, porous silicon oxide,
5 polyimide, polyimide siloxane, polysilsequioxane polymer,
6 benzocyclobutene, paralyene N, paralyene F, polyolefin,
7 poly-naphthalene, amorphous Teflon, SILK™, black diamond,
8 polymer foam, aerogel, air, dielectric gases, a partial
9 vacuum and combinations thereof.